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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,596	02/04/2004	Alfredo Herrera	16550ROUS01U	3440

34645 7590 04/26/2007

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EXAMINER	
SIEK, VUTHE	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/771,596	HERRERA, ALFREDO	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-14,16 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-14,16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/771,596 and amendment filed on 3/6/2007. Claims 1-4, 7-14 and 16-17 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 7-14, and 16-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Mason et al. (6,817,005 B2).

4. As to claim 1, Mason et al. teach a modular design method and system for programmable logic devices (see abstract, summary) comprising obtaining design implementation files (Fig. 1B); calculating a set of design output files from the design implementation files without substantial intervention from a human operator (Fig. 2B, 3B, 8B), wherein the step of calculating a set of design output files comprises the steps of initially placing logic groups (modular designs) on the programmable logic device (Fig. 1A, initial budgeting stage including run floorplanner tool); estimating the resource usage of the logic groups (sizes, shapes and position of modules on the PLD; at least see Fig. 1A-E; col. 2 lines 58—67, col. 3 lines 1-32; col. 8 lines 45-55; col. 9 lines 18-31;

col. 10 lines 30-65); estimating timing for the placed and sized logic groups (at least see col. 12 lines 35-67; col. 13 lines 1-56); and filling the logic groups with primitive information (at least see col. 12 lines 35-67; col. 13 lines 1-56); and wherein the design implementation files comprising a hollowed netlist (netlist for each module; at least see col. 12 lines 61-67) and design constraints (at least see col. 13 lines 1-55), and wherein the step of initially placing logic groups comprising merging the hollowed netlist with the design constraints, and iterating until the placement of the logic groups meets the design constraints using adjusted values without substantial intervention from a user (at least see col. 13 lines 57-67; col. 14 lines 1-67; col. 15 lines 25; col. 21 lines 54-67; col. 22 lines 1-67; col. 18 lines 60-67, col. 19 lines 1-9).

5. As to claim 14 and 16-17, remarks set forth in rejection of claim 1 equally apply because of substantially the same claim. In addition, Mason et al. a modular design method and system for programmable logic devices including translation of file into a format usable to program a programmable logic device (at least see col. 6).

6. As to claim 2, Mason et al. the design implementation files comprising a filled netlist (a netlist of complete design), and data-path constraints (top-level timing constraint when all modules are assembled) (at least see col. 6).

7. As to claim 3, Mason et al. teach the design implementation files (Fig. 1B) are not configured to directly program the programmable logic devices, and wherein the design output files are configured to program the programmable logic devices (Fig. 2B, 3B, 8B).

8. As to claim 4, Mason et al. teach generating a set of scripts (different file format shown in col. 5-6), setup files (described in col. 5-6), and tool lineup files (different tool used for programmable logic devices) for use in programming the programmable logic devices (see also files in Fig. Fig. 2B, 3B, 8B, 4-5, 8A used for programming logic devices).

9. As to claim 7, Fig. 1A shows design is divided into modules for initial placement (list of logic groups; see also Fig. 8B) and Fig. 1D-E shows list of area groups.

10. As to claim 8, Mason et al. teach estimating the resource usage of the logic groups comprising merging the filled netlist and data-path constraints and iterating until the size of logic groups is resolved (this is described in active module phase).

11. As to claim 9, Mason et al. teach analyzing the area usage to the programmable logic device and choosing an appropriate programmable logic device based on the usage analysis (this is done by mapper and floorplanner tool; Fig. 1A, 3A, 5).

12. As to claim 10, Mason et al. teach estimating timing for the placed and sized logic groups comprising merging the hollowed netlist with the data-path constraints and performing a timing analysis on the merged hollowed netlist and data-path constraints to obtain an acceptable timing margin (at least see Fig. 4).

13. As to claim 11, Mason et al. teach filling the logic groups (active modules) with primitive information comprising merging the filled netlists, design constraints, and area groups, and running the filled design to verify that it will meet the design constraints (at least see Fig. 4, 5 and 8A).

14. As to claim 12, Mason et al. teach the programmable logic device is a Field Programmable Gate Array (col. 1 lines 14-35; col. 2 lines 2-15).

15. As to claim 13, Mason et al. teach the design implementation files are files generated from Hardware Descriptor Language (HDL) files that have been subject to Register Transfer Language (RTL) Synthesis (col. 6, Fig. 1A; col. 9 lines 32-40). Note that RTL is art inherent.

Remarks

16. Applicants argued that Mason et al. does not teach automated process as recited without substantially intervention from a user. Examiner disagrees. Mason et al. teach using automated software tool (at least see Fig. 4-5). Note that the software tool is run automatically without substantially intervention from a user. Mason et al. teach if the design defects are relatively minor, then the user can use a tool named fpga_editor to manipulate individual CLBs and routing resources (col. 18 lines 30-34). Therefore, Mason et al. teach using automated software tool without substantially intervention from a user to implement an IC design on FPGA. Applicants acknowledged that it was possible to automate the process of designing a programmable logic device by causing design software to iterate design calculations using slightly different values without substantial intervention from a user until the placement of logic groups meets design constraints. Therefore, the claimed invention is not novel.

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

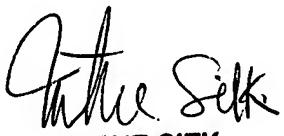
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



VUTHE SIEK
PRIMARY EXAMINER